CLAIMS

What is claimed is:

1. A method of making a semiconductor device, comprising:

providing a carbon-doped silicon oxide dielectric layer overlying a substrate;

forming a silicon carbide-based barrier layer to cover exposed surfaces of said carbon-doped silicon oxide dielectric layer;

converting a portion of said silicon carbide-based barrier layer with an oxidation treatment into a layer of silicon oxide; and

using said carbon-doped silicon oxide dielectric layer as a stop layer to remove said layer of silicon oxide.

2. A method of making a semiconductor device, comprising:

providing a silicon carbide-based barrier layer on a substrate; and

converting a portion of said silicon carbide-based barrier layer with an oxidation treatment into a layer of silicon oxide.

3. A method of making an interconnect structure, comprising:

forming a low-k dielectric layer on a substrate, said dielectric layer having at least one opening;

forming a conformal first barrier layer over exposed surfaces of said opening;

converting said first barrier layer above said dielectric layer and over the bottom of said opening into a second barrier layer, said second barrier layer having a removal rate associated with a first etchant that is greater than a removal rate of said first barrier layer associated with said first etchant; and

using said first etchant to remove said second barrier layer.

4. The method of claim 3, further comprising:

filling said opening with a conductive material; and

removing a portion of said conductive material to form a recessed conductive layer within said dielectric layer.

5. The method of claim 4, further comprising:

forming a third barrier layer on surfaces of said recessed conductive layer, said first barrier layer and said dielectric layer;

converting said third barrier layer above said dielectric layer into a fourth barrier layer, said fourth barrier layer having a removal rate associated with a second etchant that is greater than a removal rate of said third barrier layer associated with said second etchant; and

using said second etchant to remove said fourth barrier layer whereby said third barrier layer encapsulating said recessed conductive layer.

6. A method of fabricating a dielectric barrier layer in an integrated circuit structure comprising:

providing a low-k dielectric layer on a substrate, said low-k dielectric layer having at least one opening exposing an underlying metal layer; and

forming a first silicon carbide-based barrier layer to conformally cover exposed surfaces of said opening.

7. The method of claim 6, wherein said low-k dielectric layer includes carbon-doped silicon oxide.

8. The method of claim 6, wherein said first silicon carbide-based barrier layer is formed, at least in part, using a chemical vapor deposition process or a plasma enhanced chemical vapor deposition process.

9. The method of claim 8, wherein said first silicon carbide-based barrier layer is formed to a thickness of from about 200 angstroms to about 400 angstroms.

10. The method of claim 8, wherein said first silicon carbide-based barrier layer is formed at a temperature of from about 350 °C to about 450 °C.

11. The method of claim 6, further comprising:

converting said first silicon carbide-based barrier layer above said low-k dielectric layer and over the bottom of said opening with an oxidation treatment into a layer of silicon oxide.

12. The method of claim 11, wherein said oxidation treatment is a reactive oxidation treatment performed at a temperature of from about 350 °C to about 450 °C, a pressure of from about 4.0Torr to about 6.0Torr, and a radio frequency power of from about 2000W to about 3000W.

13. The method of claim 12, wherein said oxidation treatment uses a gas mixture selected from the group consisting of O_2, O_3, and N_2O.

14. The method of claim 11, further comprising:

removing said silicon oxide layer above said low-k dielectric layer and from the bottom of said opening.

15. The method of claim 14, wherein said silicon oxide layer is removed by an HF wet etching solution.

16. The method of claim 14, further comprising sequentially:

filling said opening with a conductive layer in electrical contact with said underlying metal layer;

removing said conductive layer above said low-k dielectric layer to a predetermined depth below said low-k dielectric layer to define a recess therebelow; and

forming a second silicon carbide-based barrier layer to cover said recess and above said low-k dielectric layer and said first silicon carbide-based barrier layer so as to encapsulate said conductive layer.

17. The method of claim 16, wherein said opening is filled with said conductive layer by electrochemical deposition.

18. The method of claim 16, wherein said conductive layer is removed by a chemical-mechanical planarization process.

19. The method of claim 16, wherein said second silicon carbide-based barrier layer is formed using at least one of either a chemical vapor deposition process or a plasma enhanced chemical vapor deposition process.

20. The method of claim 19, wherein said second silicon carbide-based barrier layer is formed to a thickness of from about 200 angstroms to about 400 angstroms.

21. The method of claim 19, wherein said second silicon carbide-based barrier layer is formed at a temperature of from about 350 °C to about 450 °C.

22. The method of claim 14, further comprising sequentially:

filling said opening with a layer of copper or copper alloy in electrical contact with said underlying metal layer;

removing said layer of copper or copper alloy above said low-k dielectric layer to a predetermined depth below said low-k dielectric layer to define a recess therebelow; and

forming a second silicon carbide-based barrier layer to cover said recess and above said low-k dielectric layer and said first silicon carbide-based barrier layer so as to encapsulate said layer of copper or copper alloy.

23. The method of claim 22, wherein said opening is filled with said layer of copper or copper alloy by electrochemical deposition.

24. The method of claim 22, wherein said layer of copper or copper alloy is removed by a chemical-mechanical planarization process.

25. The method of claim 16, further comprising:

converting said second silicon carbide-based barrier layer above said low-k dielectric layer with an oxidation treatment into a layer of silicon oxide; and

removing said layer of silicon oxide.

26. The method of claim 25, wherein said oxidation treatment is a reactive oxidation treatment performed at a temperature of from about 350 °C to about 450 °C, a pressure of from about 4.0Torr to about 6.0Torr, and a radio frequency power of from about 2000W to about 3000W.

27. The method of claim 26, wherein said oxidation treatment uses a gas mixture selected from the group consisting of O_2, O_3, and N_2O.

28. The method of claim 25, wherein said layer of silicon oxide is removed by an HF wet etching solution.

29. A method of fabricating a dielectric barrier layer in an integrated circuit structure comprising:

providing a low-k dielectric layer on a substrate, said low-k dielectric layer having at least one opening exposing an underlying metal layer;

forming a first silicon carbide-based barrier layer to conformally cover the exposed surfaces of said opening;

converting said first silicon carbide-based barrier layer above said low-k dielectric layer and over the bottom of said opening with an oxidation treatment into a layer of silicon oxide;

removing said silicon oxide layer above said low-k dielectric layer and from the bottom of said trench;

filling said opening with a conductive layer in electrical contact with said underlying metal layer;

removing said conductive layer above said low-k dielectric layer to a predetermined depth below said low-k dielectric layer to define a recess therebelow;

forming a second silicon carbide-based barrier layer to cover said recess and above said low-k dielectric layer and said first silicon carbide-based barrier layer so as to encapsulate said conductive layer;

converting said second silicon carbide-based barrier layer above said low-k dielectric layer with an oxidation treatment into a layer of silicon oxide; and

removing said layer of silicon oxide.

30. A semiconductor device comprising:

a low-k dielectric layer on a substrate, said low-k dielectric layer having at least one opening exposing an underlying metal layer; and

conformal silicon carbide-based barrier layers formed on the inside sidewalls of said low-k dielectric layer;

a conductive layer filled partially in said opening up to a predetermined height, said conductive layer in electrical contact with said underlying metal layer; and

a conformal second silicon carbide-based barrier layer formed above said conductive layer and coplanar with the upper surface of said low-k dielectric layer so as to encapsulate said conductive layer.

31. The semiconductor device of claim 30, wherein said low-k dielectric layer includes carbon-doped silicon oxide.

32. The semiconductor device of claim 30, wherein said first silicon carbide-based barrier layer has a thickness of from about 200 angstroms to about 400 angstroms.

33. The semiconductor device of claim 30, wherein said conductive layer includes copper or copper alloy.

34. The semiconductor device of claim 30, wherein said second silicon carbide-based barrier layer has a thickness of from about 200 angstroms to about 400 angstroms.

35. A method of fabricating a dielectric barrier layer in an integrated circuit structure, comprising:

providing a first low-k dielectric layer on a substrate having at least one opening, said opening having a via hole which exposes an underlying metal layer surrounded by said first low-k dielectric layer, said first low-k dielectric layer having an etch stop layer formed thereupon, and a trench over said via hole surrounded by a second low-k dielectric layer; and

forming a first silicon carbide-based barrier layer to conformally cover the exposed surfaces of said opening.

36. The method of claim 35, wherein said etch stop layer includes silicon carbide-based material.

37. The method of claim 35, wherein said first low-k dielectric layer includes carbon-doped silicon oxide.

38. The method of claim 35, wherein said second low-k dielectric layer includes carbon-doped silicon oxide.

39. The method of claim 35, wherein said first silicon carbide-based barrier layer is formed using at least one of either a chemical vapor deposition process or a plasma enhanced chemical vapor deposition process.

40. The method of claim 39, wherein said first silicon carbide-based barrier layer is formed to a thickness of from about 200 angstroms to about 400 angstroms.

41. The method of claim 39, wherein said first silicon carbide-based barrier layer is formed at a temperature of from about 350 °C to about 450 °C.

42. The method of claim 35, further comprising:

converting said first silicon carbide-based barrier layer above said second low-k dielectric layer, said etch stop layer, and over the bottom of said via hole with an oxidation treatment into a layer of silicon oxide.

43. The method of claim 42, wherein said oxidation treatment is a reactive oxidation treatment performed at a temperature of from about 350 °C to about 450 °C, a pressure of from about 4.0Torr to about 6.0Torr, and a radio frequency power of from about 2000W to about 3000W.

44. The method of claim 43, wherein said oxidation treatment uses a gas mixture selected from the group consisting of O_2, O_3, N_2O.

45. The method of claim 42, further comprising:

removing said silicon oxide layer above said second low-k dielectric layer and said etch stop layer, and from the bottom of said via hole.

46. The method of claim 45, wherein said silicon oxide layer is removed by an HF wet etching solution.

47. The method of claim 45, further comprising sequentially:

filling said via hole and said trench with a conductive layer in electrical contact with said underlying metal layer;

removing said conductive layer above said second low-k dielectric layer to a predetermined depth below said second low-k dielectric layer to define a recess therebelow; and

forming a second silicon carbide-based barrier layer to cover said recess and above said second low-k dielectric layer and said first silicon carbide-based barrier layer so as to encapsulate said conductive layer.

48. The method of claim 47, wherein said via hole and said trench is filled with said conductive layer by electrochemical deposition.

49. The method of claim 47, wherein said conductive layer is removed by a chemical-mechanical planarization process.

50. The method of claim 47, wherein said second silicon carbide-based barrier layer is formed using at least one of chemical vapor deposition process and plasma enhanced chemical vapor deposition process.

51. The method of claim 50, wherein said second silicon carbide-based barrier layer is formed to a thickness of from about 200 angstroms to about 400 angstroms.

52. The method of claim 50, wherein said second silicon carbide-based barrier layer is formed at a temperature of from about 350 °C to about 450 °C.

53. The method of claim 45, further comprising sequentially:

filling said via hole and said trench with a layer of copper or copper alloy in electrical contact with said underlying metal layer;

removing said copper or copper alloy layer above said second low-k dielectric layer to a predetermined depth below said second low-k dielectric layer to define a recess therebelow; and

forming a second silicon carbide-based barrier layer to cover said recess and above said second low-k dielectric layer and said first silicon carbide-based barrier layer so as to encapsulate said copper or copper alloy layer.

54. The method of claim 53, wherein said via hole and said trench is filled with said layer of copper or copper alloy by electrochemical deposition.

55. The method of claim 53, wherein said layer of copper or copper alloy is removed by a chemical-mechanical planarization process.

56. The method of claim 57, further comprising:

converting said second silicon carbide-based barrier layer above said second low-k dielectric layer with an oxidation treatment into a layer of silicon oxide; and

removing said layer of silicon oxide.

57. The method of claim 56, wherein said oxidation treatment is a reactive oxidation treatment performed at a temperature of from about 350 °C to about 450 °C, a pressure of from about 4.0Torr to about 6.0Torr, and a radio frequency power of from about 2000W to about 3000W.

58. The method of claim 57, wherein said oxidation treatment uses a gas mixture selected from the group consisting of O_2, O_3, N_2O.

59. The method of claim 56, wherein said layer of silicon oxide is removed by an HF wet etching solution.

60. A method of fabricating a dielectric barrier layer in an integrated circuit structure, comprising:

providing a first low-k dielectric layer on a substrate having at least one opening, said opening including a via hole which exposes an underlying metal layer surrounded by said first low-k dielectric layer, said first low-k dielectric layer having

an etch stop layer formed thereupon, and a trench over said via hole surrounded by a second low-k dielectric layer;

forming a first silicon carbide-based barrier layer to conformally cover the exposed surfaces of said opening;

converting said first silicon carbide-based barrier layer above said second low-k dielectric layer, said etch stop layer, and over the bottom of said via hole with an oxidation treatment into a layer of silicon oxide;

removing said silicon oxide layer above said second low-k dielectric layer and said etch stop layer, and from the bottom of said via hole;

filling said via hole and said trench with a conductive layer in electrical contact with said underlying metal layer;

removing said conductive layer above said second low-k dielectric layer to a predetermined depth below said second low-k dielectric layer to define a recess therebelow;

forming a second silicon carbide-based barrier layer to cover said recess and above said second low-k dielectric layer and said first silicon carbide-based barrier layer so as to encapsulate said conductive layer;

converting said second silicon carbide-based barrier layer above said second low-k dielectric layer with an oxidation treatment into a layer of silicon oxide; and

removing said layer of silicon oxide.

61. A semiconductor device comprising:

a first low-k dielectric layer on a substrate having at least an opening, said opening having a via hole which exposes an underlying metal layer surrounded by said first low-k dielectric layer, said first low-k dielectric layer having an etch stop layer formed thereupon, and a trench over said via hole surrounded by a second low-k dielectric layer; and

conformal silicon carbide-based barrier layers formed on the inside sidewalls of said first low-k dielectric layer, said second low-k dielectric layer and said etch stop layer.

62. The semiconductor device of claim 61, wherein said first low-k dielectric layer includes carbon doped silicon oxide.

63. The semiconductor device of claim 61, wherein said second low-k dielectric layer includes carbon doped silicon oxide.

64. The semiconductor device of claim 61, wherein said etch stop layer includes silicon carbide-based material.

65. The semiconductor device of claim 61, wherein said silicon carbide-based barrier layers have a thickness of from about 200 angstroms to about 400 angstroms.

66. A semiconductor device comprising:

a first low-k dielectric layer on a substrate having at least an opening, said opening having a via hole which exposes an underlying metal layer surrounded by said first low-k dielectric layer, said first low-k dielectric layer having an etch stop layer formed thereupon, and a trench over said via hole surrounded by a second low-k dielectric layer;

conformal silicon carbide-based barrier layers formed on the inside sidewalls of said first low-k dielectric layer, said second low-k dielectric layer and said etch stop layer;

a conductive layer completely filled in said via hole and partially filled in said trench up to a predetermined height, said conductive layer in electrical contact with said underlying metal layer; and

a conformal second silicon carbide-based barrier layer formed above said conductive layer and coplanar with the upper surface of said second low-k dielectric layer so as to encapsulate said conductive layer.

67. The semiconductor device of claim 66, wherein said first low-k dielectric layer includes carbon doped silicon oxide.

68. The semiconductor device of claim 66, wherein said second low-k dielectric layer includes carbon doped silicon oxide.

69. The semiconductor device of claim 66, wherein said etch stop layer includes silicon carbide-based material.

70. The semiconductor device of claim 66, wherein said first silicon carbide-based barrier layers have a thickness of from about 200 angstroms to about 400 angstroms.

71. The semiconductor device of claim 66, wherein said conductive layer includes copper or copper alloy.

72. The semiconductor device of claim 66, wherein said second silicon carbide-based barrier layer has a thickness of from about 200 angstroms to about 400 angstroms.

73. A method of forming a damascene structure, comprising:

forming a dielectric layer on a metal layer of a substrate, said dielectric layer having at least one opening exposing said metal layer;

forming a first barrier layer to conformally cover the exposed surfaces of said at least one opening;

providing an anisotropic treatment to convert said first barrier layer into a second barrier layer on the top surfaces of said at least one opening and over the bottom of said opening, said second barrier layer having a different etching rate from said first barrier layer;

removing said second barrier layer; and

filling said at least one opening with a conductive material.

74. A method of making an interconnect structure, comprising:

forming a low-k dielectric layer on a substrate, said first dielectric layer having a first trench;

lining the exposed surfaces of said first trench with a conformal first barrier layer;

converting said first barrier layer above said first dielectric layer and over the bottom of said first trench into a second barrier layer, such that the removal rate of said first barrier layer is higher than said second barrier layer when using a first prescribed etchant;

using said first prescribed etchant to remove said second barrier layer;

forming a first recessed conductive layer within said trench;

forming on said first recessed conductive layer a third barrier layer;

forming a second dielectric layer on said first dielectric layer, said first barrier layer, and said third barrier layer;

etching a via into said second dielectric layer and said third barrier layer such that the surface of said first recessed conductive layer is exposed;

etching a second trench into said second dielectric layer;

lining said via, second trench and the upper surface of said second dielectric layer with a fourth barrier layer;

converting said fourth barrier layer above said second dielectric layer and over the bottom of said via and second trench into a fifth barrier layer, such that the removal rate of the fourth barrier layer is higher than said fifth barrier layer when using a second prescribed etchant;

using said second prescribed etchant to remove the fifth barrier layer;

forming a second recessed conductive layer within said via and second trench; and

forming on said second recessed conductive layer a sixth barrier layer.